WISOL 와이솔

SPECIFICATION

PBA RF Module

Customer	.
Model name	**WIT300A**
Part name	**WSWIT300A00**
Date	**May 18, 2016**
Revision	**01**
Application	**WIFI IOT Module**

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1. Revision history

No.	Revision	Record Of Revision	Remarks	Revision Page
1	REV00	Initial Release	2016-05-18	-

2. Overview

The WSWIT300A00 WI-FI module provides a highly-integrated and flexible platform for developing and evaluating products and applications based on the QCA4010 SoC.

This Module includes the following components:

- QCA4010 chip
- An integrated Balun to save cost and size, minimize tuning and tolerance
- A printed antenna
- Apple MFI
- 2MB SPI Flash memory and etc.

The QCA4010 is a single chip 1x1 802.11 b/g/n device optimized for a low-power embedded applications with single-stream capability for both Tx and Rx. It has an integrated network processor with a large set of TCP/IP with IPv4/IPv6-based services. These services can be accessed via a serial SPI link or by a UART link connected to an external host CPU.

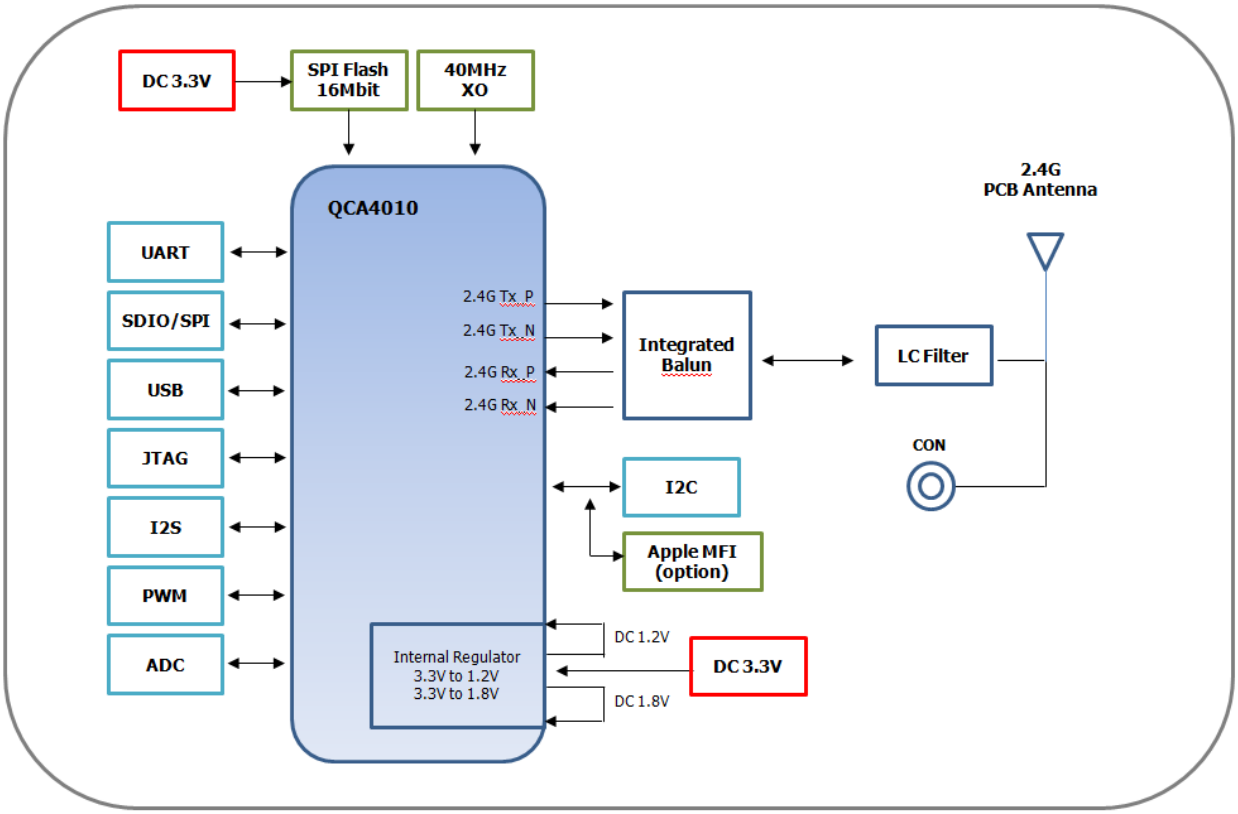

Figure 1-1 WIT300A block diagram

WIT300A Wi-Fi link features

- IEEE802.11 b/g/n, single stream 1x1
- Single-band 2.4 GHz
- Integrated PA and LNA; support for external PA and external LNA
- Gree Tx power saving mode
- Low power Listen mode
- Four-layerPCB design
- Pre-certifiedFCC
- Data rates up to 150Mbps
- Full security support: WPS, WEP,TKIP, WPA (personal), WPA2 (personal)

WIT300A Wi-Fi link features

- USB 2.0 interface with integrated controller and PHY for manufacturing test and configuration

WIT300A host interfaces

- SPI slave interface to the MCU. Host driver source code and programming APIs are available.
- UART host interface to a remote microcontroller with an AT style command set.

3. Hardware specification

3.1 Module pin assignment

Table 3-1 WIT300A Pin assignment and descriptions

Pin assign name	Pin	Type	Description
USB_DP	26	Analog IO	USB device / manufacturing test and configuration interface
USB_DN	27	Analog IO	
CHIP_PWD#	19	Digital I	Power down control signal. Setting this pin low forces the module in to its lowest power state
WAKEUP	20	Digital I	Wakeup control. In SUSPEND state, the QCA4010 monitors this pin. Once a falling or rising edge is detected, the resume sequence from SUSPEND is started.
GPIO_IOE1	29		
ADC1	40		
ADC0	41		
WIFI_HSUART_TXD	2	Digital IO	GPIO with multiplexed functions. See table 3-2 for details
WIFI_HSUART_RXD	3	Digital IO	
WIFI_HSUART_CTS	4	Digital IO	
WIFI_HSUART_RTS	5	Digital IO	
PWM7	6	Digital IO	
PWM6	7	Digital IO	

PWM5_I2CS_SDA0	8	Digital IO	
PWM4_I2CS_SCK0	9	Digital IO	
PWM0	10	Digital IO	
PWM2	11	Digital IO	
SPI_MISO_SDIO_D0_UART2_RTS	13	Digital IO	
SPI_CLK_SDIO_CLK_UART2_CTS	14	Digital IO	
SPI_INT_SDIO_D1_UART2_RXD	15	Digital IO	
SDIO_D2_UART2_TXD	16	Digital IO	
SPI_MOSI_SDIO_D3	17	Digital IO	
SPI_CS_SDIO_CMD	18	Digital IO	
SPIM_CS	30	Digital IO	
WIFI_I2S_MCLK1	32	Digital IO	
WIFI_I2S_WS1	33	Digital IO	
WIFI_I2S_SDO1	34	Digital IO	
WIFI_I2S_SDI1	35	Digital IO	
WIFI_I2S_BLK1	36	Digital IO	
ADC6_UART_R	38	Digital IO	
ADC7_UART_T	39	Digital IO	
I2CM_SDA0	43	Digital IO	
I2CM_SCL0	44	Digital IO	
EXT_ANT		RF	single-ended antenna connection
GND	1,12,21,24,25,28, 31,37,42,45,46	Power	Ground
3.3V	22,23	Power	Analog 3.3V supply

3.2 GPIO pin functions

Table 3-2 GPIO pin functions

Pin	Bootstrap	Alt1	Alt2	Alt3
2		High speed UART TXD		
3		High speed UART RXD		
4		High speed UART CTS		
5		High speed UART RTS		
6		PWM7		
7		PWM6		
8		PWM5	I2C Slave SDA0	
9		PWM4	I2C Slave SCK0	
10		PWM0		
11		PWM2		
13		SPI MISO (master or slave)	SDIO Data0	UART RTS
14		SPI CLK (master or slave)	SDIO CLK	UART CTS
15		SPI Interrupt (slave)	SDIO Data1	UART RXD
16			SDIO Data2	UART TXD
17		SPI MOSI (master or slave)	SDIO Data3	
18		SPI CS (master or slave)	SDIO Command	

19	CHIP_PWD_L			
20	IOT_MODE_EN			
30		Flash memory /CS pin		
32		I2S MCLK1		
33		I2S WS1		
34		I2S SDO1		
35		I2S SDI1		
36		I2S BLK1		
38		ADC6		
39		ADC7		
43		I2C Master SDA0		
44		I2C Master SCL0		

3.3 Module signal descriptions

3.3.1 Bootstrap signals

Table 3-3 Bootstrap signals

Signal name	Direction while CHIP_PWD# is low	Description	
IOT_MODE_EN	I	Keep high always, for normal function	
TEST_MODE,	I	Should be low while reset released, for normal function	
HM[1:0]	I	Bootstrap for host interface selection. Default mode is 00.	
		00	USB / manufacturing test and configuration / hostless
		01	Hostless (serial AT command) mode
		10	SPI host mode
		11	SDIO host mode

3.3.2 SPI slave signals

Table 3-4-1 SPI slave signals

Signal name	Direction	Description
SPI_CLK	I	Clock line from master, maximum rate 48MHz

SPI_CS	I	Chip select, active low
SPI_INT	O	Active low interrupt to SPI master controller
SPI_MIMO	O	Serial data to master
SPI_MOSI	I	Serial data from master

Table 3-4-2 SPI slave timing constraints (48MHz reference clock)

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	-	ns
t_{WH}	Clock high time	8.3	-	ns
t_{TLH}	Clock rise time	-	2	ns
t_{THL}	Clock fall time	-	2	ns
t_{ISU}	Input setup time	5	-	ns
t_{IH}	Input hold time	5	-	ns
t_{O_DLY}	Output delay	0	5	ns

3.3.3 SDIO signals

Table 3-5 SDIO signals

Signal name	Direction	Description
SD_CLK	I	SDIO clock from host
SD_CMD	IO	SDIO command line
SD_D0	IO	SDIO data lines
SD_D1	IO	
SD_D2	IO	
SD_D3	IO	

3.3.4 I2S signals

Table 3-6 I^{2}S port 0 signals

Signal name	Direction	Description	
I2S0_BCK	I	Stereo clock	
I2S0_MCK	I	Master clock	
I2S0_SDI	I	Serial data in	
I2S0_SDO	O	Serial data out	
I2S0_WS	O	Word select for stereo	
		0	Left
		1	Right

Table 3-7 I2S port 1 signals

Signal name	Direction	Description	
I2S1_BCK	I	Stereo clock	
I2S1_MCK	I	Master clock	
I2S1_SDI	I	Serial data in	
I2S1_SDO	O	Serial data out	
I2S1_WS	O	Word select for stereo	
		0	Left
		1	Right

3.3.5 I2C signals

Table 3-8 I^2C signals

Signal name	Direction	Description
I2C_CLK	lO	I^2C clock
I2C_DATA	lO	I^2C data

3.3.6 UART signals

Table 3-9 UART port0 signals

Signal name	Direction	Description
UART0_CTS	l	UART clear to send signal
UART0_RTS	O	UART ready to send signal
UART0_RXD	l	UART receive data
UART0_TXD	O	UART transmit data

Table 3-10 UART port1 signals

Signal name	Direction	Description
UART1_RXD	l	UART receive data
UART1_TXD	O	UART transmit data

3.3.7 JTAG signals

Table 3-11 JTAG signals

Signal name	Direction	Description
TCK	l	JTAG clock
TDI	I	JTAG data I
TDO	O	JTAG data O
TMS	I	JTAG mode select
TRST	I	Warm reset

3.4 Electrical characteristics

3.4.1 General DC electrical characteristics

Table 3-12 DC electrical characteristics for digital I/Os

**T_{amb} = 25 °C, VDD33 = 3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level I voltage	-	1.8	-	3.6	V
V_{IL}	Low Level I voltage	-	-0.3	-	0.3	V
V_{OH}	High Level O voltage	-	2.2	-	3.3	V
V_{OL}	Low Level O voltage	-	0	-	0.4	V

3.4.2 RX characteristics

Table 3-13 RX characteristics for 2.4GHz operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	RX input frequency range	-	2.412	-	2.472	GHz
S_{rf}	**Sensitivity**					
	CCK	1Mbps	-	-93	-	dBm
		11Mbps	-	-87	-	
	OFDM	6Mbps	-	-89	-	
		54Mbps		-73		
	HT20	MCS0	-	-89	-	
		MCS7	-	-70	-	
R_{adj}	**Adjacent channel rejection**					
	CCK	2Mbps	-	47	-	dB
	OFDM	6Mbps	-	36	-	
		54Mbps	-	21	-	
	HT20	MCS0	-	34	-	
		MCS7		18		

3.4.3 TX characteristics

Table 3-15 TX characteristics for 2.4GHz operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	TX input frequency range	-	2.412	-	2.472	GHz
P_{out}	**Output Power**					
	802.11b mask compliant	1Mbps	-	19.0	-	dBm
	802.11g mask compliant	6Mbps	-	19.0	-	
	802.11g EVM compliant	54Mbps	-	16.0	-	
	802.11n HT20 mask compliant	MCS0	-	19.0	-	
	802.11n HT20 EVM compliant	MCS7	-	15.0	-	

3.5 Throughput performance

Table 3-17 Throughput, hosted and hostless operations

	TCP uplink	TCP downlink	UDP uplink	UDP downlink	Unit
Hostless operation					
11b	5.312	5.521	6.125	6.709	Mbps
11g	19.976	18.797	23.568	31.710	
11ng HT20	25.616	21.970	37.080	40.090	
11na HT20	25.600	20.392	35.792	39.389	

3.6 Typical power consumption

Table 3-18 typical current consumption at 3.3V

Mode	State	Typical current consumption, (11ng HT20)	Unit
Standby	Suspend	168.48	uA
	Sleep (between beacon)	7.08	mA
DTIM 1	PS enabled LPL disabled	9.08	mA
DTIM 3		7.41	mA
DTIM 5		7.31	mA
DTIM 10		7.48	mA
Connection idle	PS disabled	75.16	mA
Active, TCP link	TCP uplink	130.72	mA
	TCP downlink	94.14	mA
Active, UDP uplink	Green Tx enabled	182.69	mA
	Green Tx disabled	183.16	mA
Active, UDP downlink	LPL enabled	73.65	mA
	LPL disabled	79.79	mA

4. Mechanical interface specification

4.1 Module dimensions

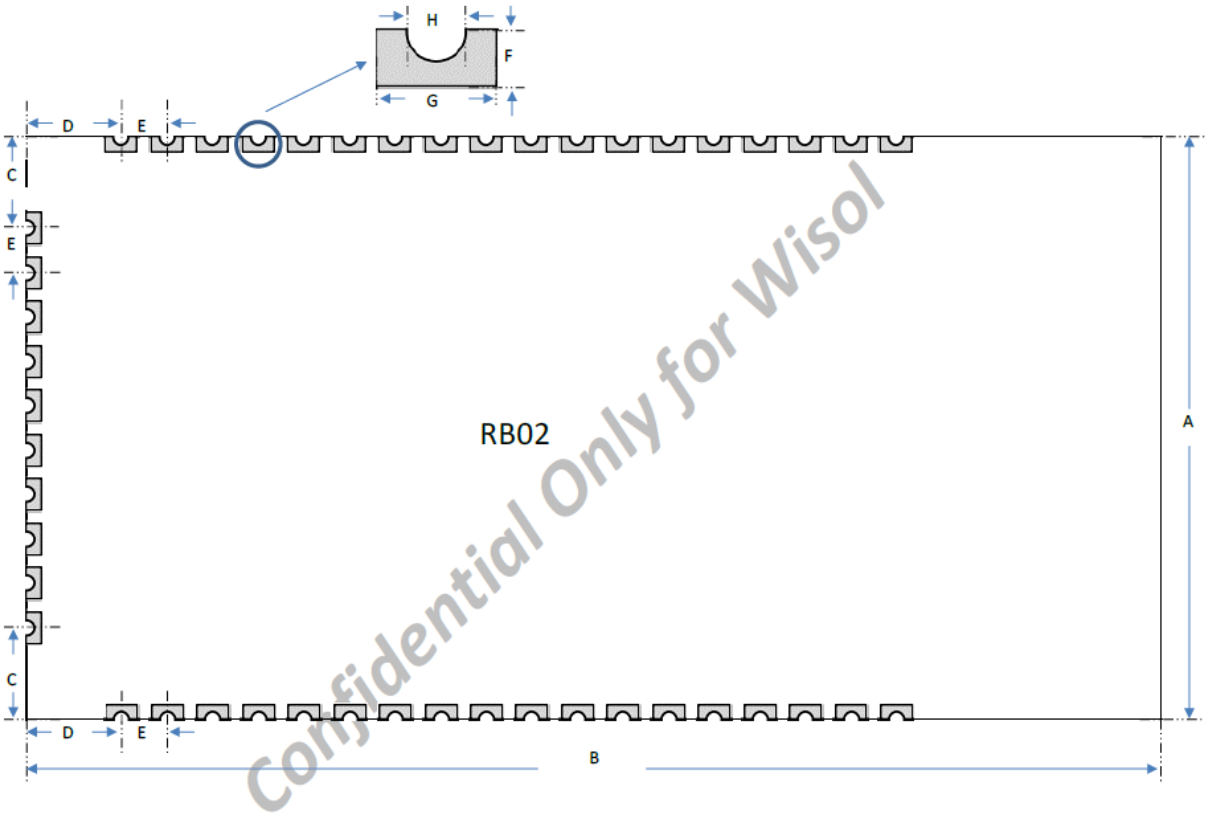

Table 4-1 Module dimensions

Dimension label	Dimension (mm)
A	16
B	30
C	2.285
D	2.54
E	1.27
F	0.4
G	0.7
H	0.5
Module height (including the RF shield)	2.6
Total height(with a coax cable plugged into the U.FL connector)	3.6